IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Awaka et al	Art Unit: 2193
Serial No.: 09/963,480	Confirmation No.: 8718
Filed: September 27, 2001	Examiner: Chat C. Do
	Docket: TI-33253

For: MULTIPLY-ACCUMULATE MODULES AND PARALLEL MULTIPLIERS AND METHODS FOR DESIGNING MULTIPLY-ACCUMULATE

Appeal Brief under 37 C.F.R. §41.37

Board of Patent Appeals and Interferences
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This is Appellant's Appeal Brief filed pursuant to 37 C.F.R. §41.37 and the Notice of Appeal filed June 14, 2007.

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Real Party in Interest

The real party in interest in this application is Texas Instruments Incorporated, a corporation of Delaware with its principle place of business in Dallas, Texas. An assignment to Texas Instruments Incorporated is recorded at reel 012210 and frames 0316 to 0319.

Related Appeals and Interferences

There are no appeals of interferences related to this appeal in this application.

Status of the Claims

Claims 1, 10, 19 and 20 are rejected and subject to this appeal. Claims 3 and 12 are allowable except for dependence upon rejected base claims. Claims 2, 4 to 9, 11 and 13 to 18 are canceled.

Status of Amendments Filed After Final Rejection

No amendments to the claims were proposed following the FINAL REJECTION of March 13, 2007.

Summary of Claimed Subject Matter

The subject matter of independent claims 1, 10, 19 and 20 of this application is taught in the application as follows.

1. A multiply-accumulate module comprising:	multiply-accumulate module 100 paragraphs [0002], [0008], [0009], [0011], [0020], [0023], [0025], [0031], [0033], [0034], [0036]
a multiply-accumulate core, wherein said multiply-accumulate core comprises:	multiply-accumulate core 120 paragraphs [0003], [0009], [0011], [0020], [0022]. [0023], [0024], [0025], [0036]

a plurality of Booth encoder cells;	Booth encoder cells 104 paragraphs [0003], [0009] to [0012], [0020] to [0025], [0036]
a plurality of Booth decoder cells connected to at least one of said Booth encoder cells; and	Booth decoder cells 110 paragraphs [0003] to [0005], [0008] to [0012], [0020], [0021], [0024], [0025], [0036]
a plurality of Wallace tree cells connected to at least one of said Booth decoder cells;	Wallace tree cells 112 paragraphs [0003] to [0005], [0008] to [0012], [0020] to [0025], [0036]
wherein said multiply-accumulate module includes a plurality of electrical paths which further include at least one critical path, said at least one critical path being an electrical path for which an amount of time that it takes for an electrical signal to travel from an input of said multiply-accumulate core to an output of said multiply-accumulate core is greater than or equal to a predetermined amount of time and less than a longest amount of time that it takes any other electrical signal to travel from said input of said multiply-accumulate core to said output of said multiply-accumulate core, wherein said predetermined amount of time is less than said longest amount of time;	plural electrical paths paragraphs [0004], [0031] critical paths paragraphs [0004], [0031]

said plurality of Booth decoder cells includes at least one first Booth decoder cell and at least one second Booth decoder cell, each of said at least one first Booth decoder cell structurally the same as each of said at least one second Booth decoder cells except that at least one of a first plurality of transistors of said first Booth decoder cell is constructed to have a width greater than a width of a corresponding one of a second plurality of transistors of said second Booth decoder cell;	first Booth decoder cell 110a1 paragraphs [0005], [0009] to [0012], [0034] to [0036] second Booth decoder cell 110a2 paragraphs [0005], [0009] to [0012], [0034] to [0036]
said plurality of Wallace tree cells including at least one first Wallace tree cell and at least one second Wallace tree cell, each of said at least one first Wallace tree cell structurally the same as each of said at least one second Wallace tree cell except that at least one of a first plurality of transistors of said first Wallace tree cell is constructed to have a width greater than a width of a corresponding one a second plurality of transistors of said second Wallace tree cell;	first Wallace tree cell 112a1 paragraphs [0005], [0009] to [0012], [0032], [0033], [0036] second Wallace tree cell 112a2 paragraphs [0005], [0009] to [0012], [0032], [0033], [0036]
wherein said at least one first Wallace tree cell and said at least one first Booth decoder cell are disposed on said at least one critical path; and	first Wallace tree cells paragraph [0032] first Booth decoder cells paragraph [0034]
wherein said at least one second Wallace tree cell and said at least one second Booth decoder cell are disposed on an electrical path not said at least one critical path and are not disposed on any of said at least one critical path.	second Wallace tree cells paragraphs [0032], [0033] second Booth decoder cells paragraphs [0034], [0035]

10. A parallel multiplier comprising:	parallel multiplier 300 paragraphs [0008], [0010] [0012], [0026], [0028], [0030], [0037]
a multiply-accumulate core, wherein said multiply-accumulate core comprises:	multiply-accumulate core 320 paragraphs [0003], [0010], [0012], [0026] to [0030], [0037]
a plurality of Booth encoder cells;	Booth encoder cells 304 paragraphs [0026] to [0030]
a plurality of Booth decoder cells connected to at least one of said Booth encoder cells; and	Booth decoder cells 310 paragraphs [0026], [0027], [0028], [0034]
a plurality of Wallace tree cells connected to at least one of said Booth decoder cells;	Wallace tree cells 312 paragraphs [0026], [0027], [0029], [0030], [0032]
wherein said parallel multiplier includes a plurality of electrical paths which further include at least one critical path, said at least one critical path being an electrical path for which an amount of time that it takes for an electrical signal to travel from an input of said parallel multiplier core to an output of said parallel multiplier core is greater than or equal to a predetermined amount of time and less than a longest amount of time that it takes any other electrical signal to travel from said input of said parallel multiplier core to said output of said parallel multiplier core, wherein said predetermined amount of time is less than said longest amount of time;	plural electrical paths paragraphs [0004], [0031] critical paths paragraphs [0004], [0031]

said plurality of Booth decoder cells includes at least one first Booth decoder cell and at least one second Booth decoder cell, each of said at least one first Booth decoder cell structurally the same as each of said at least one second Booth decoder cells except that at least one of a first plurality of transistors of said first Booth decoder cell is constructed to have a width greater than a width of a corresponding one of a second plurality of transistors of said second Booth decoder cell;	first Booth decoder cell 110a1 paragraphs [0005], [0009] to [0012], [0034] to [0036] second Booth decoder cell 110a2 paragraphs [0005], [0009] to [0012], [0034] to [0036]
said plurality of Wallace tree cells including at least one first Wallace tree cell and at least one second Wallace tree cell, each of said at least one first Wallace tree cell structurally the same as each of said at least one second Wallace tree cell except that at least one of a first plurality of transistors of said first Wallace tree cell is constructed to have a width greater than a width of a corresponding one a second plurality of transistors of said second Wallace tree cell;	first Wallace tree cells paragraph [0032] first Booth decoder cells paragraph [0034]
wherein said at least one first Wallace tree cell and said at least one first Booth decoder cell are disposed on said at least one critical path; and	first Wallace tree cells paragraph [0032] first Booth decoder cells paragraph [0034]
wherein said at least one second Wallace tree cell and said at least one second Booth decoder cell are disposed on an electrical path not said at least one critical path and are not disposed on any of said at least one critical path.	second Wallace tree cells paragraphs [0032], [0033] second Booth decoder cells paragraphs [0034], [0035]

19. A method of designing a multiply-accumulate module comprising the steps of:	multiply-accumulate module 100 paragraphs [0002], [0008], [0009], [0011], [0020], [0023], [0025], [0031], [0033], [0034], [0036], [0037]
providing a multiply-accumulate core, wherein the step of providing a multiply-accumulate core comprises the steps of:	multiply-accumulate core 120 paragraphs [0003], [0009], [0011], [0020], [0022]. [0023], [0024], [0025], [0036]
providing a plurality of Booth encoder cells;	Booth encoder cells 104 paragraphs [0003], [0009] to [0012], [0020] to [0025], [0036]
connecting a plurality of Booth decoder cells to at least one of said Booth encoder cells;	Booth decoder cells 110 paragraphs [0003] to [0005], [0008] to [0012], [0020], [0021], [0024], [0025], [0036]
connecting a plurality of Wallace tree cells to at least one of said Booth decoder cells;	Wallace tree cells 112 paragraphs [0003] to [0005], [0008] to [0012], [0020] to [0025], [0036]
defining a predetermined amount of time greater than zero and less than a longest amount of time that it takes any electrical signal to travel from said input of said multiply-accumulate core to said output of said multiply-accumulate core;	predetermined time paragraphs [0004], [0031]

defining at least one critical path within said multiply-accumulate module, said at least one critical path being an electrical path for which an amount of time that it takes for an electrical signal to travel from an input of said multiply-accumulate core to an output of said multiply-accumulate core is greater than or equal to said predetermined amount of time and less than said longest amount of time ;	critical paths paragraphs [0004], [0031]
defining a first Wallace tree cell and a second Wallace tree cell, each of said first Wallace tree cell structurally the same as each of said second Wallace tree cell except that at least one of a first plurality of transistors of said first Wallace tree cell is constructed to have a width greater than a width of a corresponding one a second plurality of transistors of said second Wallace tree cell;	first Wallace tree cell 112a1 paragraphs [0005], [0009] to [0012], [0032], [0033], [0036] second Wallace tree cell 112a2 paragraphs [0005], [0009] to [0012], [0032], [0033], [0036]
defining a first Booth decoder cell and a second Booth decoder cell, each of said first Booth decoder cell structurally the each of same as said second Booth decoder cell except that at least one of a first plurality of transistors of said first Booth decoder cell is constructed to have a width greater than a width of a corresponding one of a second plurality of transistors of said second Booth decoder cell;	first Booth decoder cell 110a1 paragraphs [0005], [0009] to [0012], [0034] to [0036] second Booth decoder cell 110a2 paragraphs [0005], [0009] to [0012], [0034] to [0036]

disposing at least one first Wallace tree cell and at least one first Booth decoder cell on said at least one critical path;	first Wallace tree cells paragraph [0032] first Booth decoder cells paragraph [0034]
disposing at least one second Wallace tree cell and said at least one second Booth decoder cell are on an electrical path not said at least one critical path; and	second Wallace tree cells paragraphs [0032], [0033] second Booth decoder cells paragraphs [0034], [0035]
not disposing any second Wallace tree cell or any second Booth decoder cell on any of said at least one critical path.	second Wallace tree cells paragraphs [0032], [0033] second Booth decoder cells paragraphs [0034], [0035]

20. A method of designing a parallel multiplier comprising the steps of:	parallel multiplier 300 paragraphs [0008], [0010] [0012], [0026], [0028], [0030], [0037]
providing a parallel multiplier core, wherein the step of providing a parallel multiplier core comprises the steps of:	multiply-accumulate core 320 paragraphs [0003], [0010], [0012], [0026] to [0030], [0037]
providing a plurality of Booth encoder cells;	Booth encoder cells 304 paragraphs [0026] to [0030]
connecting a plurality of Booth decoder cells to at least one of said Booth encoder cells;	Booth decoder cells 310 paragraphs [0026], [0027], [0028], [0034]
connecting a plurality of Wallace tree cells to at least one of said Booth decoder cells;	Wallace tree cells 312 paragraphs [0026], [0027], [0029], [0030], [0032]
defining a predetermined amount of time greater than zero and less than a longest amount of time that it takes any electrical signal to travel from said input of said parallel multiplier core to said output of said parallel multiplier core;	predetermined time paragraphs [0004], [0031]

defining at least one critical path within said parallel multiplier, said at least one critical path being an electrical path for which an amount of time that it takes for an electrical signal to travel from an input of said parallel multiplier core to an output of said parallel multiplier core is greater than or equal to said predetermined amount of time and less than said longest amount of time;	critical paths paragraphs [0004], [0031]
defining a first Wallace tree cell and a second Wallace tree cell, each of said first Wallace tree cell structurally the same as each of said second Wallace tree cell except that at least one of a first plurality of transistors of said first Wallace tree cell is constructed to have a width greater than a width of a corresponding one a second plurality of transistors of said second Wallace tree cell;	first Wallace tree cell 112a1 paragraphs [0005], [0009] to [0012], [0032], [0033], [0036] second Wallace tree cell 112a2 paragraphs [0005], [0009] to [0012], [0032], [0033], [0036]
defining a first Booth decoder cell and a second Booth decoder cell, each of said first Booth decoder cell structurally the same as each of said second Booth decoder cell except that at least one of a first plurality of transistors of said first Booth decoder cell is constructed to have a width greater than a width of a corresponding one of a second plurality of transistors of said second Booth decoder cell;	first Booth decoder cell 110a1 paragraphs [0005], [0009] to [0012], [0034] to [0036] second Booth decoder cell 110a2 paragraphs [0005], [0009] to [0012], [0034] to [0036]

disposing at least one first Wallace tree cell and at least one first Booth decoder cell on said at least one critical path;	first Wallace tree cells paragraph [0032] first Booth decoder cells paragraph [0034]
disposing at least one second Wallace tree cell and at least one second Booth decoder cell are on an electrical path not said at least one critical path; and	second Wallace tree cells paragraphs [0032], [0033] second Booth decoder cells paragraphs [0034], [0035]
not disposing any second Wallace tree cell or any second Booth decoder on any of said at least one critical path.	second Wallace tree cells paragraphs [0032], [0033] second Booth decoder cells paragraphs [0034], [0035]

Grounds for Rejection to be Reviewed on Appeal

Claims 1, 10, 19 and 20 were rejected under 35 U.S.C. 103(a) as made obvious by the combination of Hansen et al U.S. Published Patent Application No. 2003/0110197 and Itoh U.S. Published Patent Application No. 2001/0009012.

Arguments

Claims 1, 10, 19 and 20 recite subject matter not made obvious by the combination of Hansen et al and Itoh. Claims 1, 10, 19 and 20 recite "each of said first Booth decoder cell structurally the same as each of said second Booth decoder cell except that at least one of a first plurality of transistors of said first Booth decoder cell is constructed to have a width greater than a width of a corresponding one of a second plurality of transistors of said second Booth decoder cell" and "each of said first Wallace tree cell structurally the same as each of said second Wallace tree cell except that at least one of a first plurality of transistors of said first Wallace tree cell is constructed to have a width greater than a width of a corresponding one a second plurality of transistors of said second Wallace tree cell.". Hansen et al neither teaches a transistor difference in width of nor cells differing in any way. The FINAL REJECTION states at page 4, lines 10 to 15:

> "Hansen et al. fail to disclose at least one of the first Booth decoder cell as transistor is constructed to have a width greater than a width of a corresponding transistor of second Booth decoder cell as transistor. However, Itoh explicitly discloses at least one of the first Booth decoder cell as transistor is constructed to have a width greater than a width of a corresponding transistor of second Booth decoder cell as transistor (e.g. paragraph [0036] and [0042])."

The Applicants respectfully submit that Itoh fails to teach the differing transistor widths recited in claims 1, 10, 19 and 20. Itoh states at paragraph [0036]:

> "[0036] If the size of the component transistor (a ratio of a channel width to a channel length in the case of an MOS transistor) is increased to generate an output at high speed in each stage, the area of the multiplication array of the multiplication apparatus increases. Thus, the size of the

> component transistor is the minimum required size to increase integration degree. The third order partial product must be transmitted from the third order 4:2 addition circuit 6a to final addition circuit 7 over a distance of half the length of the multiplication array. A signal propagation delay during the transmission increases, whereby high speed multiplication cannot be achieved."

This portion of Itoh teaches selecting a transistor size as the minimum size to achieve the desired operational speed. The Applicants submit that one skilled in the art would understand from the teaching of paragraph [0036] of Itoh that all circuits have the same corresponding ratio of channel width to a channel length selected to achieve the necessary speed of operation. Itoh fails to teach making two such transistor size selections for circuits of differing locations. Without teaching the differing selection of transistor size recited in claims 1, 10, 19 and 20, Itoh fails to add to the teaching of Hansen et al to make obvious this limitation. Accordingly, claims 1, 10, 19 and 20 are allowable over the combination of Hansen et al and Itoh.

Claims 1, 10, 19 and 20 recite further subject matter not made obvious by the combination of Hansen et al and Itoh. Claims 1, 10, 19 and 20 each recite at least one critical path. As pointed out by the Examiner, Hansen et al inherently includes such critical paths as defined in claims 1, 10, 19 and 20 but does not explicitly teach critical paths. Apparatus claims 1 and 10 each recite "wherein said at least one first Wallace tree cell and said at least one first Booth decoder cell are disposed on said at least one critical path; and wherein said at least one second Wallace tree cell and said at least one second Booth decoder cell are disposed on an electrical path not said at least one critical path and are not disposed on any of said at least one critical path." Method claims 19 and 20 similarly recite "disposing at least one first Wallace tree cell and at least one first Booth decoder cell

on said at least one critical path; disposing at least one second Wallace tree cell and at least one second Booth decoder cell are on an electrical path not said at least one critical path; and not disposing any second Wallace tree cell or any second Booth decoder on any of said at least one critical path." Hansen et al fails to teach defining critical paths and the two types of cells used depend upon whether the cell is on such a critical path. Hansen et al likewise fails to teach that one type cell is used in critical paths and another type cell is used in paths not critical paths and not used in critical paths. Itoh states at paragraph [0042]:

> "[0042] In the Wallace tree type multiplication apparatus, the multiplication tree array is formed into the divided structure where multiplication is independently performed in each of the divided arrays. Thus, the length of a critical path is reduced for high speed multiplication."

This teaching of Itoh indicates that high speed operation is achieved in a different manner than recited in claims 1, 10, 19 and 20. Claims 1, 10, 19 and 20 recite differing transistor widths at differing locations so those cells on the critical paths are faster. Itoh teaches constructing the multiplication tree array in a divided structure to reduce the lengths of the critical paths. Thus teaching of Itoh adds nothing to make this limitation obvious because Itoh teaches a different technique relating to the claimed critical path. Itoh fails to teach constructing cells with differing transistor widths for differing locations within the circuit. Accordingly, claims 1, 10, 19 and 20 are allowable over the combination of Hansen et al and Itoh.

If the Examiner has any questions or other correspondence regarding this application, Applicants request that the Examiner contact Applicants' attorney at the below listed telephone number and address to facilitate prosecution.

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CLAIMS APPENDIX

1. A multiply-accumulate module comprising:

a multiply-accumulate core, wherein said multiply-accumulate core comprises:

a plurality of Booth encoder cells;

a plurality of Booth decoder cells connected to at least one of said Booth encoder cells; and

a plurality of Wallace tree cells connected to at least one of said Booth decoder cells;

wherein said multiply-accumulate module includes a plurality of electrical paths which further include at least one critical path, said at least one critical path being an electrical path for which an amount of time that it takes for an electrical signal to travel from an input of said multiply-accumulate core to an output of said multiply-accumulate core is greater than or equal to a predetermined amount of time and less than a longest amount of time that it takes any other electrical signal to travel from said input of said multiply-accumulate core to said output of said multiply-accumulate core, wherein said predetermined amount of time is less than said longest amount of time;

said plurality of Booth decoder cells includes at least one first Booth decoder cell and at least one second Booth decoder cell, each of said at least one first Booth decoder cell structurally the same as each of said at least one second Booth decoder cells except that at least one of a first plurality of transistors of said first Booth decoder cell is constructed to have a width greater than a width of a corresponding one of a second plurality of transistors of said second Booth decoder cell;

said plurality of Wallace tree cells including at least one first Wallace tree cell and at least one second Wallace tree cell, each of said at least one first Wallace tree cell structurally the

same as each of said at least one second Wallace tree cell except that at least one of a first plurality of transistors of said first Wallace tree cell is constructed to have a width greater than a width of a corresponding one a second plurality of transistors of said second Wallace tree cell;

wherein said at least one first Wallace tree cell and said at least one first Booth decoder cell are disposed on said at least one critical path; and

wherein said at least one second Wallace tree cell and said at least one second Booth decoder cell are disposed on an electrical path not said at least one critical path and are not disposed on any of said at least one critical path.

3. The multiply-accumulate module of claim 1, wherein said multiply-accumulate core further comprises:

an adder connected to at least one of said Wallace tree cells;

a saturation detector connected to said adder, wherein said multiply-accumulate module further comprises:

at least one input register connected to at least one of said Booth encoding cells; and

at least one result register connected to said saturation detector.

10. A parallel multiplier comprising:

a parallel multiplier core, wherein said parallel multiplier core comprises:

a plurality of Booth encoder cells;

a plurality of Booth decoder cells connected to at least one of said Booth encoder cells; and

a plurality of Wallace tree cells connected to at least one of said Booth decoder cells;

wherein said parallel multiplier includes a plurality of electrical paths which further include at least one critical path, said at least one critical path being an electrical path for which an amount of time that it takes for an electrical signal to travel from an input of said parallel multiplier core to an output of said parallel multiplier core is greater than or equal to a predetermined amount of time and less than a longest amount of time that it takes any other electrical signal to travel from said input of said parallel multiplier core to said output of said parallel multiplier core, wherein said predetermined amount of time is less than said longest amount of time;

said plurality of Booth decoder cells includes at least one first Booth decoder cell and at least one second Booth decoder cell, each of said at least one first Booth decoder cell structurally the same as each of said at least one second Booth decoder cells except that at least one of a first plurality of transistors of said first Booth decoder cell is constructed to have a width greater than a width of a corresponding one of a second plurality of transistors of said second Booth decoder cell;

said plurality of Wallace tree cells including at least one first Wallace tree cell and at least one second Wallace tree cell, each of said at least one first Wallace tree cell structurally the same as each of said at least one second Wallace tree cell except that at least one of a first plurality of transistors of said first Wallace tree cell is constructed to have a width greater than a width of a corresponding one a second plurality of transistors of said second Wallace tree cell;

wherein said at least one first Wallace tree cell and said at least one first Booth decoder cell are disposed on said at least one critical path; and

wherein said at least one second Wallace tree cell and said at least one second Booth decoder cell are disposed on an electrical

path not said at least one critical path and are not disposed on any of said at least one critical path.

12. The parallel multiplier of claim 10, wherein said parallel multiplier core further comprises:

an adder connected to at least one of said Wallace tree cells;

a saturation detector connected to said adder, wherein said parallel multiplier further comprises:

at least one input register connected to at least one of said Booth encoding cells; and

at least one result register connected to said saturation detector and at least one of said Wallace tree cells.

19. A method of designing a multiply-accumulate module comprising the steps of:

providing a multiply-accumulate core, wherein the step of providing a multiply-accumulate core comprises the steps of:

providing a plurality of Booth encoder cells;

connecting a plurality of Booth decoder cells to at least one of said Booth encoder cells;

connecting a plurality of Wallace tree cells to at least one of said Booth decoder cells;

defining a predetermined amount of time greater than zero and less than a longest amount of time that it takes any electrical signal to travel from said input of said multiply-accumulate core to said output of said multiply-accumulate core;

defining at least one critical path within said multiply-accumulate module, said at least one critical path being an electrical path for which an amount of time that it takes for an electrical signal to travel from an input of said multiply-accumulate core to an output of said multiply-accumulate core is

greater than or equal to said predetermined amount of time and less than said longest amount of time ;

defining a first Wallace tree cell and a second Wallace tree cell, each of said first Wallace tree cell structurally the same as each of said second Wallace tree cell except that at least one of a first plurality of transistors of said first Wallace tree cell is constructed to have a width greater than a width of a corresponding one a second plurality of transistors of said second Wallace tree cell;

defining a first Booth decoder cell and a second Booth decoder cell, each of said first Booth decoder cell structurally the each of same as said second Booth decoder cell except that at least one of a first plurality of transistors of said first Booth decoder cell is constructed to have a width greater than a width of a corresponding one of a second plurality of transistors of said second Booth decoder cell;

disposing at least one first Wallace tree cell and at least one first Booth decoder cell on said at least one critical path;

disposing at least one second Wallace tree cell and said at least one second Booth decoder cell are on an electrical path not said at least one critical path; and

not disposing any second Wallace tree cell or any second Booth decoder cell on any of said at least one critical path.

20. A method of designing a parallel multiplier comprising the steps of:

providing a parallel multiplier core, wherein the step of providing a parallel multiplier core comprises the steps of:

providing a plurality of Booth encoder cells;

connecting a plurality of Booth decoder cells to at least one of said Booth encoder cells;

connecting a plurality of Wallace tree cells to at least one of said Booth decoder cells;

defining a predetermined amount of time greater than zero and less than a longest amount of time that it takes any electrical signal to travel from said input of said parallel multiplier core to said output of said parallel multiplier core;

defining at least one critical path within said parallel multiplier, said at least one critical path being an electrical path for which an amount of time that it takes for an electrical signal to travel from an input of said parallel multiplier core to an output of said parallel multiplier core is greater than or equal to said predetermined amount of time and less than said longest amount of time;

defining a first Wallace tree cell and a second Wallace tree cell, each of said first Wallace tree cell structurally the same as each of said second Wallace tree cell except that at least one of a first plurality of transistors of said first Wallace tree cell is constructed to have a width greater than a width of a corresponding one a second plurality of transistors of said second Wallace tree cell;

defining a first Booth decoder cell and a second Booth decoder cell, each of said first Booth decoder cell structurally the same as each of said second Booth decoder cell except that at least one of a first plurality of transistors of said first Booth decoder cell is constructed to have a width greater than a width of a corresponding one of a second plurality of transistors of said second Booth decoder cell;

disposing at least one first Wallace tree cell and at least one first Booth decoder cell on said at least one critical path;

disposing at least one second Wallace tree cell and at least one second Booth decoder cell are on an electrical path not said at least one critical path; and

not disposing any second Wallace tree cell or any second Booth decoder on any of said at least one critical path.

Evidence Appendix

None

Related Proceedings Appendix

None